NEW CHIP PAIR PROVIDES ISOLATED DRIVE FOR HIGH VOLTAGE IGBTs

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Abstract

Recent advances in the design of Insulated Gate Bipolar Transistors (IGBTs) have increased their capabilities to the point where they are replacing power MOSFETs as the switching device of choice for high voltage/high current power supply and motor drive systems. Although switching speeds of IGBTs are generally slower than those of power MOSFETs, devices are now available with similar gate drive requirements. At the same time, these devices retain the inherent superior conduction characteristics of bipolar transistors. A new integrated circuit pair, the UC3726/UC3727, provides a cost-effective way to drive IGBTs in "high-side" and isolated switching applications. This application note describes the operation of this chip pair, as well as the unique problems associated with driving IGBTs. Many of the concepts presented here are similar to those presented in Unitrode Application Note U-127, written by John O'Connor, which describes the UC3724/UC3725 power MOSFET driver pair. This application note replaces Unitrode Application Note U-143 due to specification changes on the UC3727.

INTRODUCTION

IGBT OPERATION AND APPLICATIONS

While power MOSFETs have many desirable features such as high peak current capability, wide safe operating area (SOA), and ruggedness, they do have some inherent disadvantages. Among these are conduction characteristics that are strongly dependent on temperature, voltage rating and die size. Furthermore, the conduction characteristics of power MOSFETs are largely insensitive to gate voltage, and for large values of drain current, the drain to source voltage is primarily a linear function of the drain current. This effect severely limits the maximum current capability of MOSFETs since power loss is a squared function of drain current ($P_L = R_{DS} \bullet (I_D)^2$).

IGBTs, on the other hand, function more like bipolar transistors than MOSFETs. The IGBT equivalent circuit consists of a PNP transistor driven by a low voltage MOSFET in a pseudo-Darlington configuration. Since the voltage drop across the IGBT is the sum of the voltage drop across the P-N junction and the voltage drop across the driving MOSFET, the total voltage drop across the IGBT can never go below a diode drop. This leads to greater power dissipation at low current levels than for a MOSFET. However, this disadvantage is greatly offset by the fact that the conduction characteristics of IGBTs increase with increasing gate voltage. An increase in gate voltage leads to an increase in channel current for the driving MOSFET. This in turn leads to a reduction in voltage drop across the PNP. Furthermore, since the output PNP behaves largely like a bipolar transistor, voltage drop is not a linear function of collector current, which leads to much lower power dissipation at high current levels. Because of these superior characteristics, IGBTs can operate at much higher current levels than power MOSFETs of the same die size.

OVERVIEW OF IGBT DRIVE REQUIREMENTS AND PROBLEM AREAS

The conduction characteristics of an IGBT are similar to those of an N-channel MOSFET in that a positive gate-to-emitter voltage is required for conduction. This characteristic leads to the problem of gate biasing in "high-side" drive applications. Since the gate must be biased above the high voltage input, high side drive requirements can lead to costly and complex gate circuits, as the gate must sometimes be biased hundreds of volts above system ground.

In addition to the biasing problem, other gate drive requirements include low drive impedance to reduce switching losses, as well as sufficient current to charge the gate fast enough to achieve the desired switching time. The charge current requirement is derived from the total gate charge (Q_g) as specified on the IGBT data sheet. Additionally, since the combination of high voltage and relatively fast switching speed results in both high dv/dt and di/dt, the gate is usually biased with a negative voltage during turn off to prevent transient turn on.

This requirement results in added complexity for the gate drive circuitry. Finally some method must be implemented to protect the IGBT and/or other drive circuitry from damage during over current faults.

Unitrode Application Note U-127 mentions several common approaches to solving the high side driver problem. Among the common techniques used are floating power supplies for the driver circuitry, charge pump circuits, high voltage driver ICs, and optocoupler isolated driver circuits. Each of these techniques have limitations, and those limitations are discussed in detail in U-127.

UC3726/UC3727 DRIVER PAIR

The UC3726/UC3727 IC pair provides an elegant, yet compact and cost-effective solution to the problem of driving IGBTs in high side and isolated applications. The chip pair is similar to the UC3724/ UC3725 chip pair, except optimized for the unique problems associated with driving IGBTs. Figure 1 shows the basic circuit configuration for the UC3726/UC3727 circuit pair. In addition to the IC pair, a few passive components and a pulse transformer are required to complete the circuit. Also, an optocoupler can be used to provide fault information to the UC3726 if it is desired. The optocoupler can be eliminated and fault protection still provided by the UC3727 if it is not required to pass fault information back to the system. This feature is explained in detail in the fault section of this application note.

The UC3726 transmitter generates a carrier signal that utilizes a unique duty cycle modulation technique to transmit both command signal and power to the UC3727. Operating the carrier at high frequency, up to 750kHz, allows for minimum transformer cost and size. Since the high voltage isolation is provided with a magnetic element instead of silicon, two low voltage ICs can be used. This leads to a very cost effective and simple solution to the high voltage gate drive problem.

The UC3727 comparator circuitry senses the transmitted duty cycle and decodes the ON/OFF gate drive command. A diode bridge rectifies the carrier input to provide power to the IC. The output gate drive signal is in phase with the command, and is guaranteed to be 16V. Intermediate high drive or clamp levels can be programmed for various periods of time to limit surge current at turn on, and during short term fault conditions. A bipolar voltage supply is also provided to supply negative gate drive to insure that the IGBT remains off in the presence of high common mode slew rates.

UC3726 DRIVE TRANSMITTER

Figure 2 shows the block diagram for the UC3726 drive transmitter IC. The major components of the circuit include two tri-level output drivers with zero current sense detectors and control logic, a bias voltage generator with undervoltage lockout, a retriggerable one shot, a TTL compatible input with hysteresis, as well as fault sense circuitry and control logic.

The circuit operates by using a unique duty cycle modulation technique to simultaneously pass ON/OFF command information and power to the UC3727 isolated IGBT high side driver. This technique was originally developed for the UC3724/ UC3725 high side MOSFET driver pair. Application

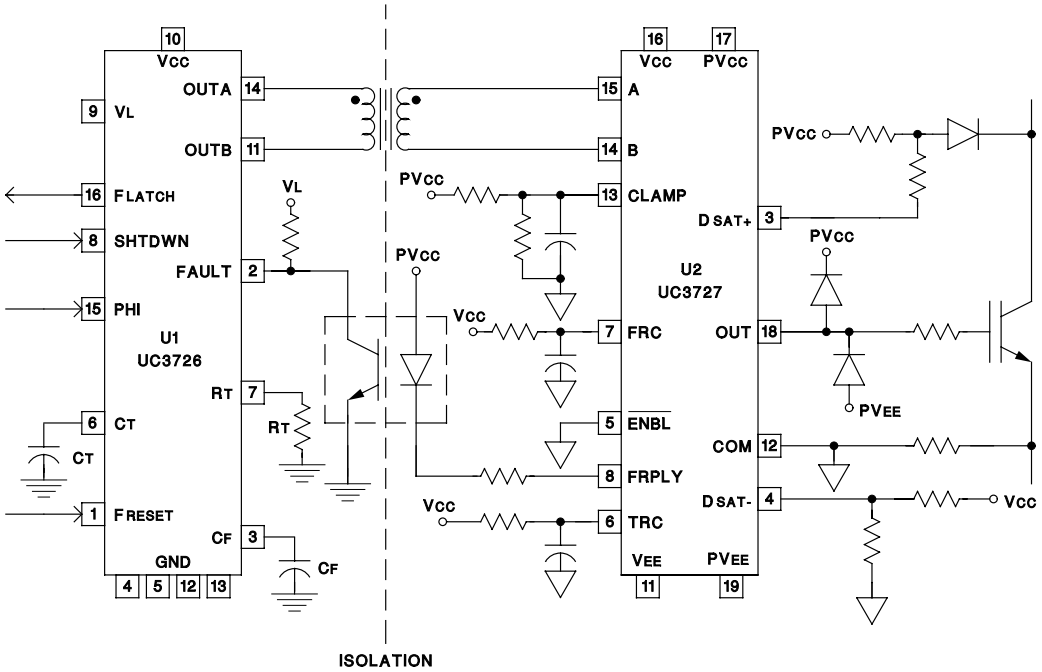

Figure 1. UC3726/UC3727 Circuit Pair

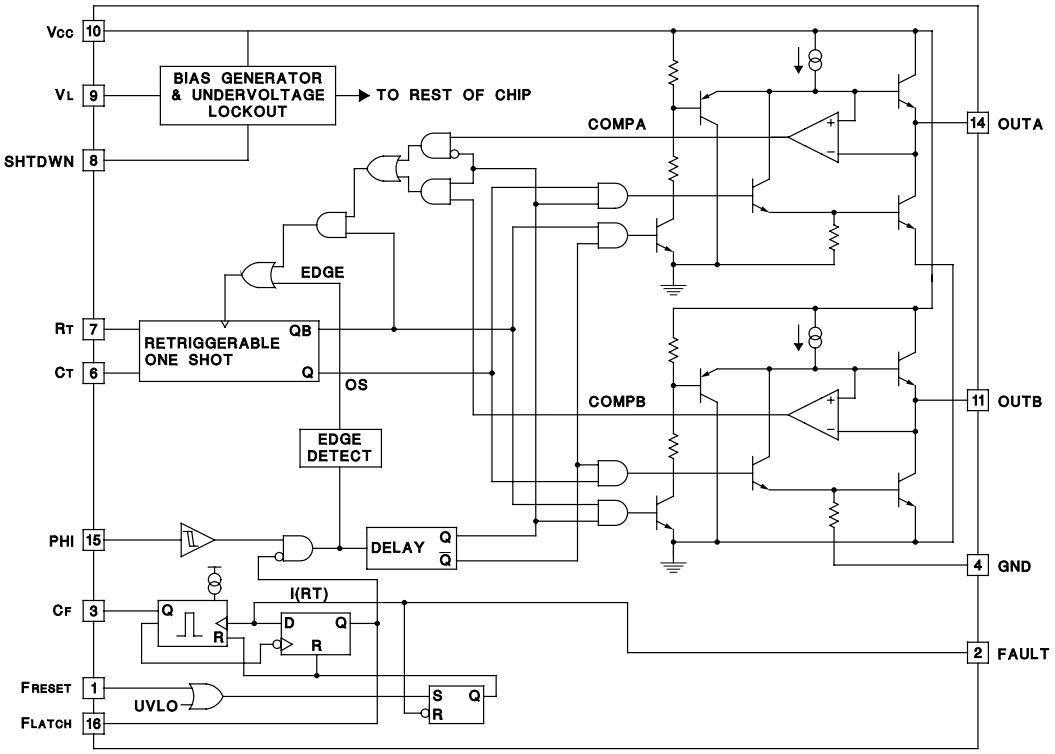

Figure 2. Drive Transmitter IC

Note U-127 describes the operation of that chip pair, and many of the concepts are similar. Specific differences primarily relate to waveform timing.

CARRIER FREQUENCY/TIMING/OUTPUT DRIVES/INPUT COMMAND

By choosing a high frequency carrier, cost efficiency can be maximized. The carrier frequency uses both a one shot pulse width and the pulse transformer reset time to set the overall period. The one shot pulse width is set by the timing resistor (R_T) and capacitor (C_T). During the one shot pulse time C_T, along with its parallel parasitic capacitance, is charged with a constant current determined by R_T and the logic voltage V_L:

1) $Ict = V_L/4R_T$

For this and all other equations in this applications note, all resistors are in ohms, all capacitors are in farads, and time is in seconds. The parasitic capacitance of approximately 50pF adds to C_T to form the total capacitance C_{TOT}. This capacitance charges from its initial value of $0.22 \bullet V_L$ until it reaches the threshold voltage of $0.5 \bullet V_L$, at which time the one-shot pulse terminates. Using the current/voltage relationship for a capacitor of I=C(dv/dt) yields the pulse width time:

2) $T_{PW} = (C_{TOT} \bullet (V_L)(0.5\text{-}0.22))/Ict = (C_{TOT} \bullet 0.25V_L \bullet 4R_T)/V_L = R_T \bullet C_{TOT} \bullet 1.1$

Notice that V_L does not appear in the final equation for T_{PW} , and therefore the tolerance on V_L does not affect the one shot period. During the one shot period "full" output voltage is applied across the primary of the pulse transformer, with one output held at V_{CC}-2.0V, and the other output held at 0.3V. During this time, transformer magnetizing current rises linearly at a rate determined by the transformer inductance and applied voltage:

3) $di/dt = (V_A\text{-}V_B)/L_{pri}$

At the end of the one shot period, the control logic reverses the polarity of the applied voltage. During this time, one output is held at $V_{CC} \bullet 0.6$, and the other output is held at V_{CC} + 0.4V. The result is a "half" voltage applied across the transformer primary which is opposite in polarity to the "full" voltage, and the core is reset. The magnetizing current decreases at a linear rate which is half of the rising rate. The outputs are held in this state until the current sense detectors determine that the current in the transformer has reached zero. At that point, the one-shot is retriggered, and the cycle repeats. Since the reset rate is half the energizing rate, the reset time is twice as long as the energizing time. The overall period for the carrier frequency is therefore:

4) $T_{CF} = 3 \bullet T_{PW}$

Power is transferred to the UC3727 only during the one shot period. During this time the primary current is the sum of the magnetizing current and the load current. Since no power is transferred during the reset period, the primary current is composed of only demagnetizing current during this time. By switching when the current in the primary reaches

zero, the UC3726 assures that the core is reset, and there is no danger of saturation.

Figure 3 shows steady state waveforms for a continuous logic low input command. At time t_0 the one shot pulse begins, and the voltage across C_T charges until it reaches the threshold at time t_1. The magnetizing current in the primary builds up linearly during this time. At t_1 the one shot period ends, and the primary current begins decreasing. At time t_2 zero current is reached and detectors retrigger the one shot, initiating the next one shot cycle. The waveforms for V_A and V_B reflect the half and full voltage concepts described previously.

The downward slope on V_{CT} is the result of an internal timing circuit which provides a blanking interval which will not allow the output drivers to switch states while the inductor current is decreasing until a time period equal to the energizing period has expired. This protection feature is provided to prevent switching transients from triggering a state change on the output drivers prematurely.

If a continuous high input is commanded, the waveforms for V_A and V_B are interchanged, and the magnetizing current is inverted. The UC3727 determines command information by sensing the polarity of the full voltage at the transformer secondary.

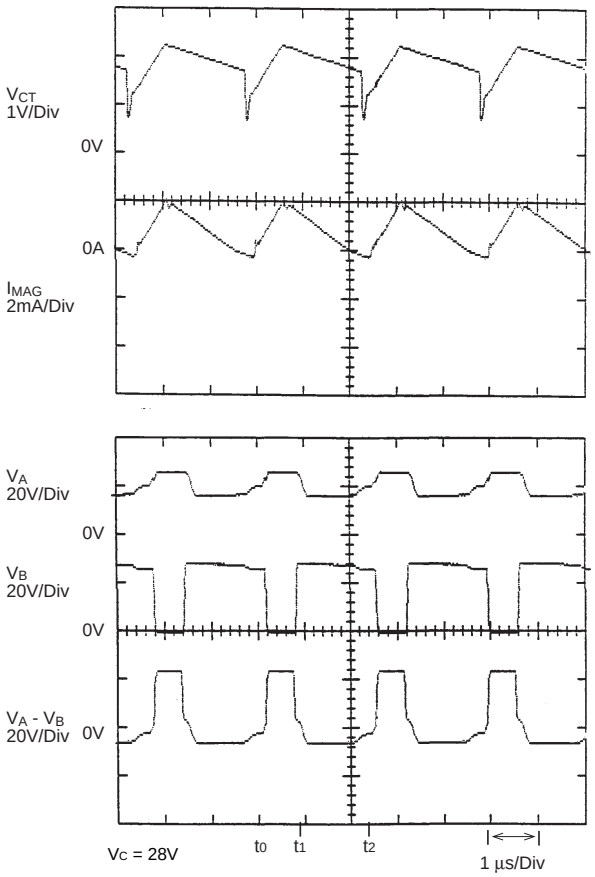

Figure 3. Steady State Waveforms Continuous Logic Low Input

This is described in detail later in this application note.

When a command transition occurs, the existing oscillator cycle is terminated, and a new cycle is started by applying full voltage in the opposite polarity. There is no danger of saturating the core, because the current must fall to zero before a new one shot trigger can occur. Newly incorporated circuitry prevents output jitter during a command transition by assuring equal propagation delay to the output regardless of the point in the cycle that the transition occurs.

FAULT/FAULT TIMING/FAULT RESET

The UC3726 contains special circuitry to prevent drive information from being transmitted during fault conditions. The FAULT input to the chip is designed to interface with the UC3727 through an optocoupler. At power up the UC3726 FAULT pin is pulled high through an external resistor, and the fault logic is reset by the UVLO circuitry.

Once its UVLO level is exceeded, the UC3727 drives the FAULT pin low, and the fault logic is enabled. After this point, the UC3727 will keep the FAULT pin low unless a fault is indicated. Special fault detection circuitry in the UC3727 detects overcurrent conditions (faults) and informs the UC3726 through the FAULT signal. To be recognized as a valid fault, the FAULT signal must remain high during the entire fault window. The timing for this window is set by C_F and R_T and is determined by the following equation:

5) $t_F = (C_F \bullet R_T) \bullet 2.1$

If a valid fault is recognized, the fault latch is set, and the outputs will remain in the logic low states until the FRESET signal (input to the UC3726) is toggled high. This signal should be powered up low, and remain low until a valid fault is recognized. Once the fault is cleared, the FRESET signal should be brought low again. The minimum pulse width on FRESET to guarantee a reset is 1µsec.

Figure 4 shows the waveforms for the FAULT circuitry signals for a valid fault. It should be noted that use of this function requires a "smart" system.

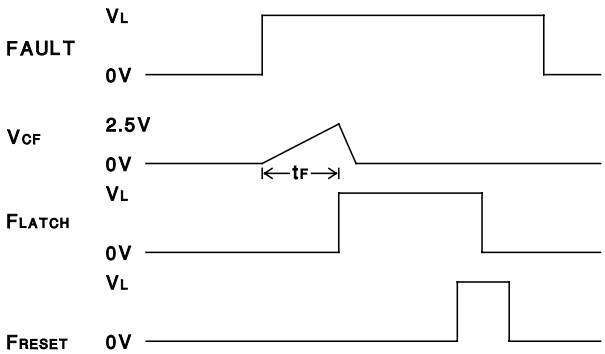

Figure 4. Fault Circuitry Signals

The fault latch must be reset in order for operation to continue once a valid fault is recognized. If the optocoupler used has a high level of output capacitance, it may be necessary to provide a reset pulse to the FRESET pin of the UC3726 after it has completed its power up sequence. Since a low to high transition on the FAULT pin indicates a valid fault, a slow rising waveform on this pin will result in a fault indication at power up. If this occurs, the output drive of the UC3726 will be latched off until the reset pulse is provided.

If this level of complexity is not desired or required, the FAULT input to the UC3726 can be permanently enabled by tying it low, allowing the UVLO circuitry to reset the fault latch. The UC3727 has additional fault protection circuitry that will protect the output IGBT independently, but the UC3726 will not be informed that a fault has occurred. Since the FAULT input to the UC3726 is tied low through a low impedance, the reset pulse after power up is not required for this case.

SHUTDOWN/UVLO/LOGIC VOLTAGE OPERATION

The UC3726 provides a shutdown pin (SHTDWN) which can be used to place the IC in a low power shutdown mode. By bringing this point high, the internal reference is disabled, and supply current is reduced to 2.5mA typical. Since the typical supply current when the chip is active is 20mA, the power savings are substantial. While in shutdown mode, both the A and B output drives are held low (ground). If an external logic supply is used, it must also be disabled for the shutdown feature to work.

The UC3726 also provides internal under voltage lockout (UVLO) circuitry. This feature will disable the internal reference, and disable the output drivers (hold at ground), if VCC is below 6.5V. It should be noted, however, that VCC must be held high enough to satisfy the UVLO feature of the UC3727. If the pulse transformer has a turns ratio of 1:1, VCC must be held at 28V to guarantee proper operation of the UC3727. This requirement is derived from the maximum saturation drops of the UC3726, as well as the UVLO, rectifier drops, and VCC specifications of the UC3727. For operation with VCC less than 28V, the turns ratio of the transformer must be adjusted to provide enough voltage to the UC3727. This requirement is explained further in the output drive section of this application note, which provides detail on pulse transformer selection and design.

The UC3726 also brings out the logic voltage supply to a separate pin. If an external logic voltage supply is used, ICC is reduced from 22mA typical to 12mA typical. Regardless of whether an external logic supply is used or not, this pin must be bypassed to ground with a high quality ceramic capacitor of at least 0.1µF.

UC3727 ISOLATED HIGH SIDE IGBT DRIVER

Figure 5 shows the block diagram of the UC3727 high side IGBT driver IC. The major circuit components include a Schottky diode rectifier bridge, a differential sense comparator with hysteresis, a bias and reference generator including undervoltage lockout circuitry and thermal shutdown, a high current gate driver stage with a programmable clamp drive level, a negative gate drive voltage supply, and fault detection and shutdown circuitry. An enable input is also provided to allow for stand alone operation with external bipolar voltage supplies.

SIGNAL AND POWER INPUT/NEGATIVE POWER SUPPLY

As shown on Figure 5, the input stage to the UC3727 both rectifies the input signal to supply power to the IC, and demodulates the input signal to determine the polarity of the gate drive command. Because the rectifier bridge peak detects the input signal, power is only transferred to the storage capacitors during the "full" voltage portion of the duty cycle. This operating mode prevents the flow of any secondary current through the pulse transformer during the "half" voltage portion of the duty cycle. The primary current is therefore composed of only demagnetizing current during the reset or "half" voltage portion of the cycle. Since the waveform is switched based on zero current detection, the transformer core is completely reset each cycle.

When "full" voltage is applied, the external storage capacitors are charged through the rectifier bridge. The energy stored in these capacitors is used to power the UC3727 circuitry, and to provide instantaneous charge to the IGBT gate during turn on. A detailed description of proper capacitor selection is provided in the decoupling section of this application note.

An internal "GND" amplifier maintains a floating common 16.5V below VCC. By referencing this common point to the emitter of the IGBT, the gate voltage can be driven to a negative voltage during turn off.

The internal hysteresis comparator of the UC3727 senses the polarity of the input command by determining the polarity of the "full" input voltage. The comparator threshold is only set or reset if the input voltage exceeds 0.95 • (VCC - VEE) or 0.95 • (VEE - VCC). The IGBT gate is turned on if the "full" voltage is positive with respect to common, and turned off if the "full" voltage is negative with respect to common. Note that this represents a logic

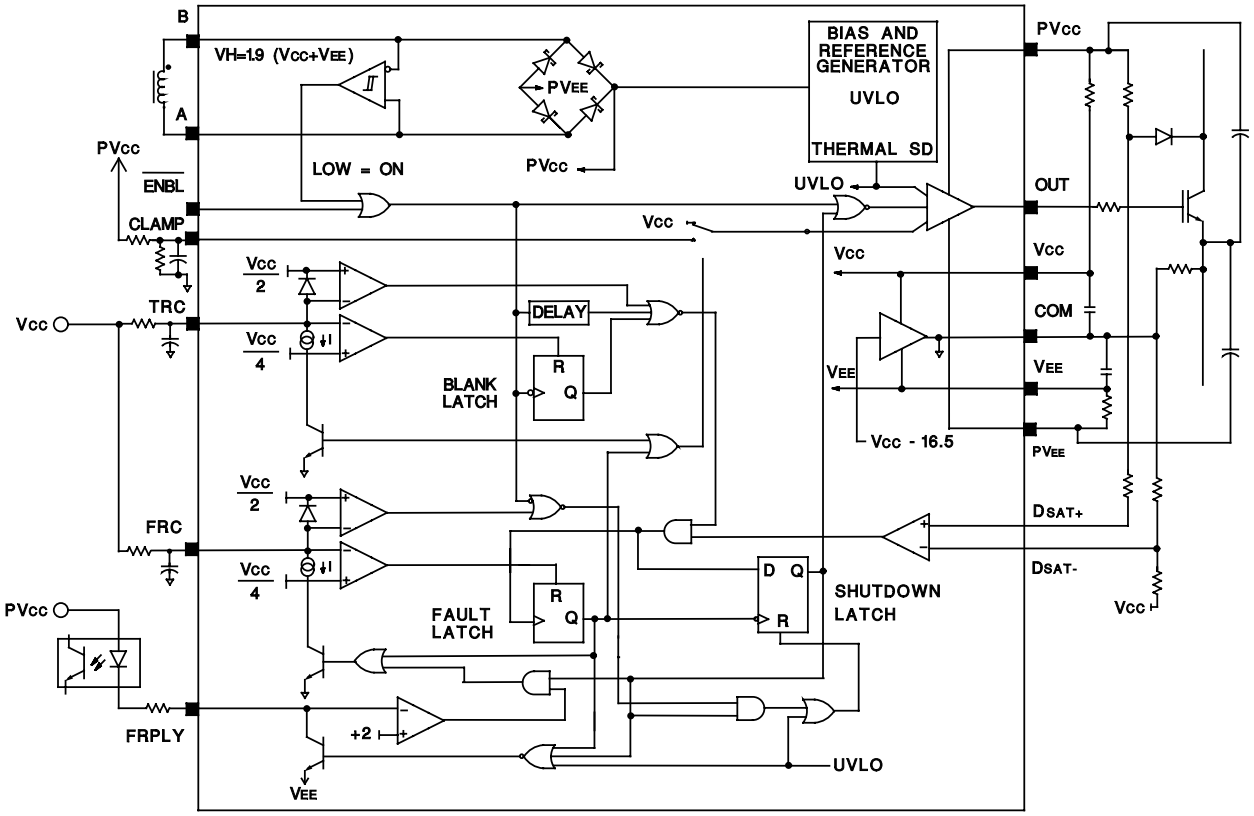

Figure 5. UC3727 High Side IGBT Driver IC

inversion to account for the logic inversion in the UC3726.

The UC3727 provides separate inputs for V_{CC}, PV_{CC}, V_{EE}, and PV_{EE}. By separating the output driver supplies (PV_{CC} and PV_{EE}) from the power supplies for the rest of the circuitry, better noise immunity can be achieved. The PV_{CC} and PV_{EE} inputs should be isolated from their respective low current supplies by 3.3Ω and bypassed to the IGBT emitter with 1.0µF capacitors as shown on Figure 5.

OUTPUT DRIVER STAGE

The output stage of the UC3727 consists of a high current, bipolar power amplifier. The peak output current of 4A provides the ability to drive IGBT gates requiring large amounts of gate charge. In order to provide a controlled or "soft" gate drive signal, the gate drive can be programmed for a two step turn on waveform. At turn on, the drive amplifier waveform will rise to a user defined clamp level for a user defined time duration. The benefits and uses of this clamp level are explained in further detail in the following section of this application note. After the time duration expires, the drive waveform will then rise to its maximum level (approximately 15V).

The common output of the UC3727 is designed to be referenced to the emitter of the IGBT to allow the gate to be driven negative during turn off. By regulating this common point to a fixed level below V_{CC}, the remaining differential supply voltage (V_{CC} - V_{EE}) - (V_{CC} - V_{COM}) can be used to generate the negative bias.

Under voltage lockout is also featured in the UC3727. Because V_{COM} is a regulated point below V_{CC}, the differential input voltage V_A - V_B must exceed the maximum potential difference between V_{CC} and V_{COM}, plus the UVLO level between V_{COM} and V_{EE}, plus the diode drops of the rectifier bridge. In equation form this can be stated as:

6) $V_A - V_B \geq V_{CC} + V_{EEUVLO} + 2V_D$

The differential input voltage is supplied by the UC3726 through the pulse transformer (in most cases). Consideration must be given to Equation 6 when selecting a supply voltage for the UC3726, and during pulse transformer selection. If worst case specifications are considered, the differential input voltage must be greater than 25.3V to guarantee proper operation of the UC3727.

OUTPUT CLAMP/SOFT TURN ON

A common application of IGBTs involves driving clamped inductive loads. In this case, the maximum allowable reverse recovery current of the clamp diode can be a limiting factor. One way to limit the reverse recovery current is to provide a soft turn on to the IGBT gate. Since the conduction

of the IGBT channel is sensitive to gate voltage, the peak current through the channel can be limited by providing a clamp level during turn on. Unfortunately, this will result in greater switching losses. Considerable care must therefore be taken when programming the clamp level and time duration. Tradeoffs must be made at the system design level between reverse recovery current limitations and switching losses.

Referring to Figure 5, the clamp level is determined by a resistive divider between V_{CC} and common. The clamp level is approximately the voltage level at the clamp input pin. As the gate voltage rises, the gate drive signal is "caught" by the clamp circuit at the clamp level. Because a significant amount of charge is rerouted through the clamp circuit at this point, the clamp pin must be bypassed to common with a high quality capacitor of at least 0.1µF, and the DC impedance of the clamp network should be limited to approximately 10k ohms.

Also referring to Figure 5, the clamp time is set by the RC network at the TRC input to the UC3727. When a command is received to turn on the gate, the gate drive circuit rises to the clamp level, and the voltage at TRC is discharged by an internal current source. Once the threshold of $V_{CC}/4$ is reached, an internal comparator trips, and full gate voltage is applied. The clamp period is determined by:

$$7)\ Tp = R_{TRC} \bullet C_{TRC} \bullet In\left(\frac{R_{TRC} - 7600}{R_{TRC} - 12400}\right)$$

This RC network also determines the blanking time for the desaturation comparator. The desaturation comparator is used to detect fault conditions which result in the IGBT coming out of saturation while the gate drive is high. Due to the turn on delay of the IGBT, this comparator must be ignored after a command transition to the on state until the IGBT transitions into saturation. The blanking time requirement is derived from the turn on and saturation characteristics of the IGBT.

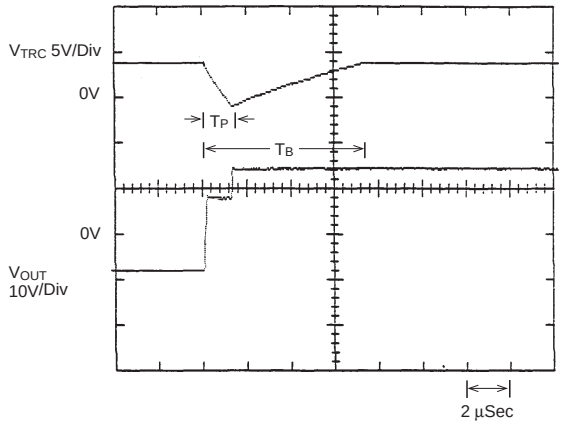

Figure 6. Gate Drive and TRC Waveforms Positive Gate Transition

Once the clamp time period has expired, the output driver increases the gate voltage to the fully on level. The voltage at TRC is then allowed to charge back to $V_{CC}/2$. The total time it takes to discharge and recharge the capacitor defines the blanking period and is determined by:

$$8)\ Tb = Tp + 0.4 \bullet R_{TRC}C_{TRC}$$

Because we have two equations and two unknowns, the clamp time and blanking time can be programmed independently. Figure 6 illustrates the gate drive waveform and the voltage at TRC during a positive gate drive transition.

FAULT/FAULT TIMING/DESATURATION AMPLIFIER

As described previously, IGBTs offer several advantages over power MOSFETs due to their superior conduction characteristics. They also exhibit several advantages over bipolar transistors and Darlingtons such as lower power dissipation and higher operating frequencies. Unfortunately, an IGBT that has been optimized for superior conduction and efficiency, is generally vulnerable to damage due to short circuits or faults. Because of their high conductivity, short circuit currents for IGBTs can be quite high, making them susceptible to damage due to excess power dissipation.

When building short circuit protection into an IGBT driver circuit, the response of the protection circuit must be fast enough to insure that the device is shut off before damage to the IGBT or any other part of the circuit occurs. At the same time, care must be taken to avoid nuisance triggering from short duration faults that do not result in any circuit damage. If the gate drive to the IGBT is shut off completely as soon as a fault is detected, the result may be an intolerable amount of nuisance shut downs. Therefore, it would be advantageous to program the allowable short circuit time as long as possible.

If the gate drive voltage is reduced when a fault is detected, the short circuit current can be reduced, and therefore the short circuit time can be stretched. However, reducing the gate voltage also increases the saturation voltage of the IGBT, which is undesirable for normal conduction. Therefore, the ideal short circuit protection technique will reduce the gate voltage only when a fault condition is detected, and keep the gate voltage at the reduced level for as long as possible, before shutting down the IGBT completely. In order for this technique to work effectively, the maximum short circuit time as a function of gate voltage must be known.

Referring again to Figure 5, the UC3727 provides a desaturation comparator designed to detect short circuit or fault conditions, and provide both short term and long term protection for the IGBT. The

DSAT+ input to the comparator is biased off to a DC level which is higher than the maximum saturation level of the IGBT plus one diode drop. During normal operation, the DSAT- input will be pulled down to the saturation voltage of the IGBT plus one diode drop. The blanking period discussed previously protects against false trips of the desaturation comparator while the IGBT is turning on.

If a fault occurs outside of the blanking interval, the gate drive will be reduced to the clamp level for a time period determined by the RC network at the FRC pin of the UC3727. The time period can be calculated by the following equation:

9) $T_f = R_{FRC} \bullet C_{FRC} \bullet ln((R - 7600)/(R - 12400))$

As soon as the fault is detected the FRPLY output of the UC3727 will go high. If the UC3726 is configured to accept this signal as an input, through an optocoupler or level shift network, its own fault timing circuitry will be activated.

If the desaturation event ends before the fault time has expired, the gate drive will be driven back to its maximum level, and FRPLY will go back low. In order to insure that the desaturation amplifier can accurately determine that a fault condition no longer exists, the DSAT- input level must be biased higher than the desaturation level of the IGBT with the reduced gate drive, plus a diode drop.

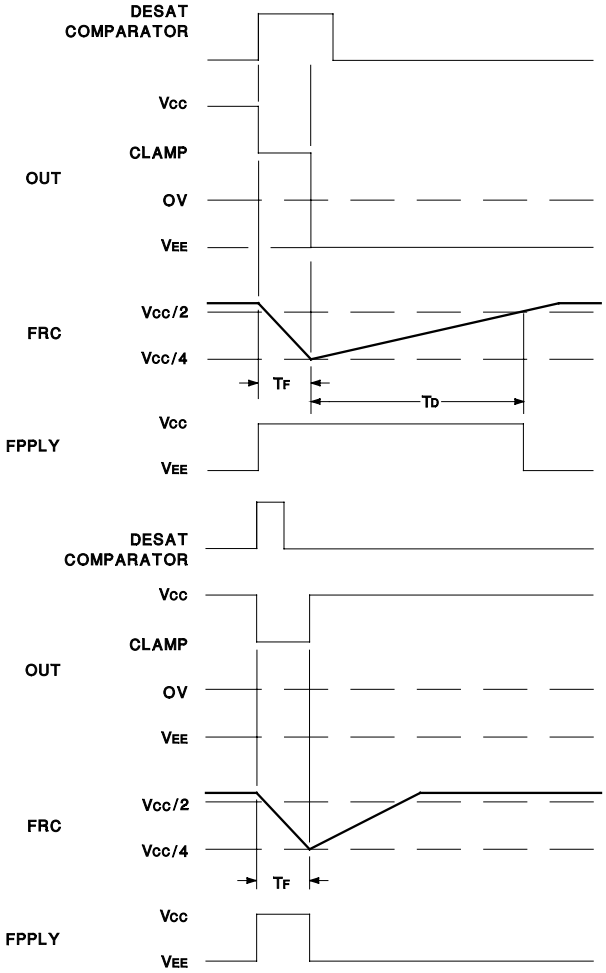

Figure 7. Fault Signal Waveforms

If the desaturation event does not end within the fault time, the output gate drive will be driven completely off, and the chip will not accept a command to drive the gate high until a delay period has expired. The equation for the delay period is determined by the same RC network as the fault time:

10) $T_d = 0.4 \bullet R_{FRC} \bullet C_{FRC}$

Again, since there are two equations and two unknowns, the fault time and delay time can be programmed independently. FRPLY will remain high for the entire delay period. If the UC3726 is configured to accept FRPLY as an input, it will have the ability to prevent any command to turn on the gate from being transmitted until its fault latch has been reset. Figure 7 shows the waveforms for fault signals for both transient and long term faults.

ENABLE INPUT/STAND ALONE OPERATION

The UC3727 provides an active low enable input for stand alone operation. This input is useful for operating the chip as a high side driver with isolated power supplies. The enable input can also be used to control the chip for low side driver applications if external power supplies are available. If the UC3727 is not used in stand alone mode, i.e. it is driven by the UC3726, the enable input should be tied to common.

If $\overline{\text{ENBL}}$ is used as a command input, the B input should be tied to VCC, and the A input should be tied to VEE. Note the polarity change described previously. The output gate drive will be driven high when $\overline{\text{ENBL}}$ is held at the same potential as common, and the gate drive will held low when $\overline{\text{ENBL}}$ is tied to VCC. For low side driver applications $\overline{\text{ENBL}}$ can be controlled by a discrete transistor operating off of conventional logic. For high side driver applications, $\overline{\text{ENBL}}$ must be controlled by an optocoupler, or a discrete transistor operating off as a level shift network. Because the optocoupler or discrete transistor will function as an inverter in this case, the result will be positive logic to the output. Therefore, turning on the optocoupler or transistor will turn on the IGBT. Figure 8 shows a circuit diagram for using the $\overline{\text{ENBL}}$ input as a command input.

If external power supplies as used for grounded emitter low side operation, common should never be connected to system ground. This point is not designed to sink the large amounts of current flowing out of the emitter of the IGBT. Both the positive and negative supplies should by bypassed to common with capacitors, and the common output should be DC isolated from ground.

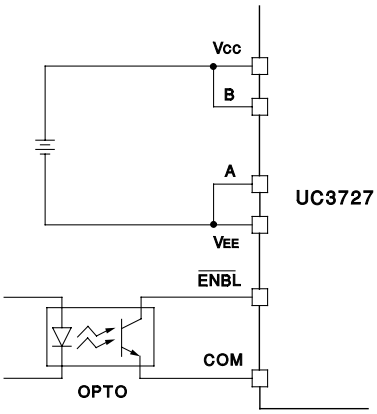

Figure 8. ENBL Used as Command Input

PRACTICAL DESIGN CONSIDERATIONS/EXAMPLE CIRCUIT

Figure 9 depicts a typical high side IGBT driver circuit. All of the features of the IC driver pair are utilized to provide maximum circuit protection and flexibility. This configuration might be used as a high side switch for a power supply, or it might form part of an H-bridge configuration for a motor driver. A resistive load is assumed in order to illustrate the high switching speeds of the driver pair. Real systems would likely require driving clamped inductive loads, and switching speed would be purposely slowed to protect external components such as clamp diodes. Component values for the support circuitry are chosen based on the specific requirements of the system. What follows is a step by step design procedure for a typical circuit.

PULSE TRANSFORMER DESIGN CONSIDERATIONS

Application note U-127 provides a detailed explanation of recommended transformer design criteria for the UC3724/UC3725 chip pair. Since the transformer design procedure is similar for the UC3726/UC3727 chip pair, the theory is not repeated in this application note. However, a transformer has been designed by Coilcraft (Q3868-A) specifically for use with the UC3726/UC3727 pair. This transformer has been optimized for operation at 400kHz, resulting in small size and low cost. Since the maximum switching frequency for the IGBT is 1/4 of the transformer frequency, the resulting 100kHz maximum IGBT frequency is near the typical maximum operating range of power IGBTs. The following calculations provide a brief overview of the design of the Q3868-A transformer:

Assuming a V_C of 30V for the UC3726 and typical total saturation drops of 2.3V for the output drivers, the resulting voltage across the transformer winding will be 27.7V. Ignoring propagation delay, and choosing a peak magnetizing

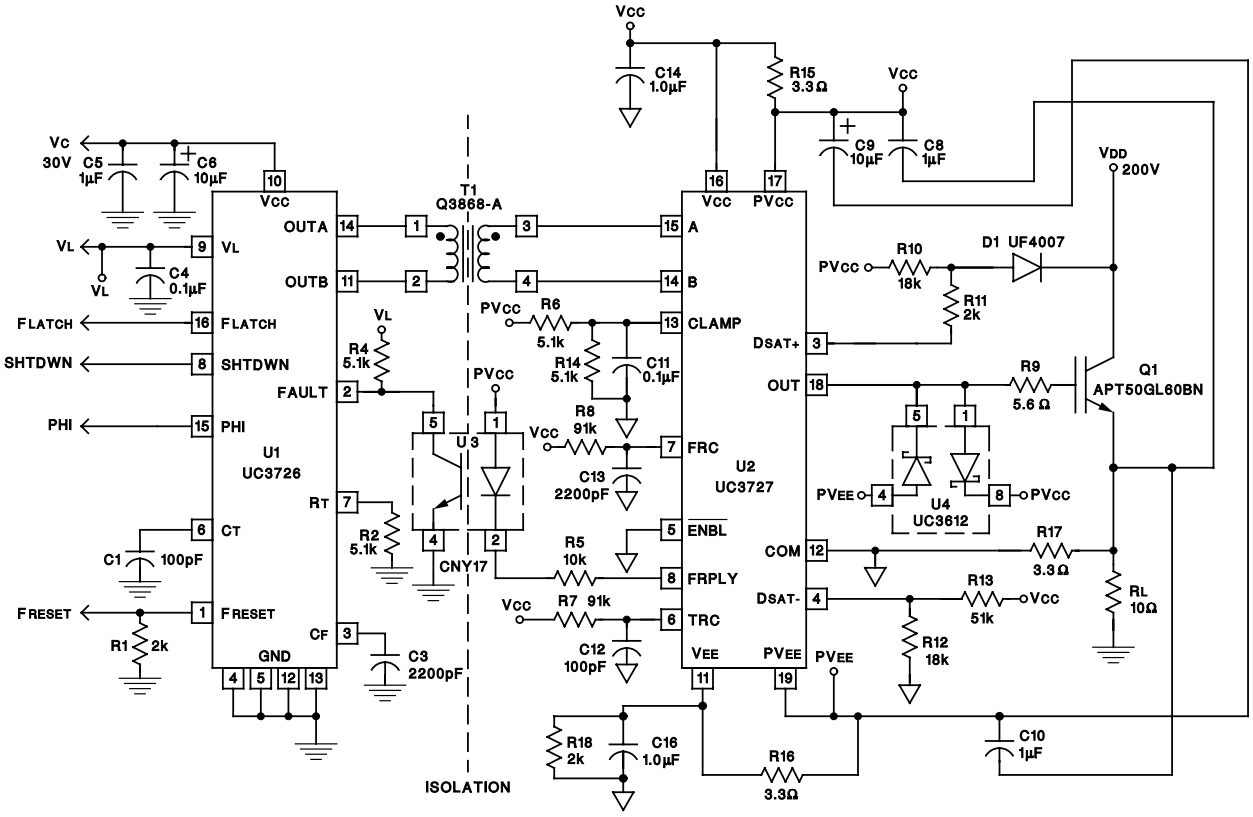

Figure 9. Typical High Side Driver Circuit

current of 35mA, the required primary inductance can be calculated using Equation 7 of U-127:

11) $L_{pri} = ((27.7V)(833ns))/0.035A = 659\mu H$

The 833ns represents 1/3 of the period of the 400kHz carrier, which is the pulse width time as defined by Equation 4 of this document:

12) $T_{PW} = 1/(3 \bullet 400kHz) = 833ns$

Using Equation 8 of U-127, and an initial value of A_L = 2000mH/1000 turns, an estimated number of turns is calculated:

13) $N_{TURNS} = ((659\mu H \bullet 10^9)/2000)^{1/2} = 18$ turns

From Equation 8 of U-127:

14) $A_e = ((27.7V)(833ns)(10^4)/((18\ turns)(0.05T)) = 0.256\ cm^2$

A Magnetics core, P-41206-TC was chosen with the following specifications:

A_L = 2820mH/1000 turns

A_e = 0.221 cm^2

V_e = 0.554 cm^3

Recalculating the number of turns yields:

15) $N_{TURNS} = ((659\mu H)(10^9)/2820)^{1/2} = 15.3$ turns, use 15 turns

The flux density of the transformer design is then checked using Equation 8 of U-127:

16) $delta\ B = ((27.7V)(833ns)(10^4)/((15\ turns)(0.221\ cm^3) = 0.069T$

To determine the core loss due to the magnetizing current, the core loss vs. flux density curve for the core is consulted:

At 400kHz and 0.069T, P_L = 400mW/cm^3

Therefore, the core loss can be calculated as:

17) $P_{CL} = (400mW/cm^3)(0.554\ cm^3) = 222mW$

The transformer is wound with AWG #30 KYNAR wire. In order to minimize leakage inductance, the primary and secondary windings are wound bifilar. The maximum DC resistance of the primary winding is 0.130 ohms, and therefore resistive losses due to magnetizing current are minimal. There will be additional resistive losses due to bias current for the UC3727 and gate drive current for the IGBT. For IGBTs with large gate charge requirements, these losses may become significant, and the transformer design must be adjusted accordingly.

In some cases it may be necessary to add a damping resistor across the transformer secondary to minimize ringing and eliminate false triggering of the hysteresis comparator.

Once the transformer design has been completed, and an operating frequency has been chosen, the values for R_T and C_T can be selected. Since a wider selection of resistors is available than capacitors, we choose C_T = 100pf. We then use Equation 2 and a one shot pulse width of 833ns to determine R_T :

18) $R_T = (833ns)/((100pF + 50pF) \bullet 1.1) = 5.1k$

Referring to Figure 9, this results in R2 = 5.1k and C1= 100pF.

OUTPUT DRIVE CONSIDERATIONS/CLAMP LEVEL AND BLANKING TIME

In order to design the gate drive portion of the IGBT driver circuit, several criteria must be considered to balance what sometimes are conflicting requirements. The ideal situation would involve switching the IGBT as fast as possible to minimize switching losses. However, there will be cases when it is desirable to reduce the switching speed of the IGBT. An example case would be slowing down the turn on time to limit the reverse recovery current into the free wheel diode when driving a clamped inductive load. Another example might be reducing the turn on time in a half bridge configuration to prevent cross conduction.

In order to evaluate the drive requirements of the IGBT, the gate charge characteristics of the device are used. However, evaluating the gate charge does not lead to a good prediction of switching times as it does with power MOSFETs. The reason for this is the fact that IGBTs are minority carrier devices. This characteristics leads to slower switching times than power MOSFETs due to base charge storage. The turn off time is much slower than the turn on time, and is characterized by a "tail" in the current waveform. To predict switching times of IGBTs, the manufacturers data sheets must be consulted for turn on delay (t_d on), rise time (t_r), turn off delay (t_d off), and fall time t_f.

The drive circuitry should be designed so that additional delay is not introduced due to gate charge requirements. In the example shown in Figure 9, an APT50GL60BN IGBT is used (500V, 60A). The key timing specifications of this device are as follows:

Total Gate Charge (Q_g) = 110nC

Turn On Delay (t_d on) = 15ns

Rise Time (t_r) = 50ns

Turn Off Delay (t_d) = 55ns

Fall Time (t_f) = 350ns

The UC3727 output stage is a 4A peak driver. The time required to charge the gate is therefore:

19) $T_{CH} = 110nC/4A = 27.5ns$

Since this time is about half of the sum of the turn on delay time and the rise time, significantly reducing the drive current will slow down the turn on time of the device. However the fall time of the IGBT is much longer (350ns), and therefore gate drive current does not significantly affect the turn off time.

For the example circuit it is assumed that the fastest switching speed possible is desired. However, since the UC3727 is rated for 4A peak drive current, a gate resistor is used to limit the peak current. Taking into account rectifier and saturation drops, the maximum swing of the gate voltage is 20.5 volts. The gate resistor is therefore chosen by:

20) *R9 = 21.5V/4A = 5.1ohm, use 5.6ohm*

For circuits like half bridge amplifiers where cross conduction is a concern, a diode can be used with dual gate resistors to provide a higher gate impedance for turn on than for turn off, to provide cross conduction protection. An example of this technique is shown in the design example section of this application note.

For circuits where the collector of the IGBT is subjected to high dv/dt, the gate resistor must be sufficiently small to prevent unwanted gate turn on due to voltage drop across the gate resistor when current flows through the Miller capacitance in the presence of the high dv/dt. For high current IGBTs, emitter inductance can also cause transient turn on in the presence of high di/dt, by pulling the emitter node negative. These problems are partially mitigated by the negative gate bias of the gate drive in the off state, but the designer must be aware of the additional limitations in gate resistor selection if large values of gate resistors are desired.

For large IGBTs the power rating of the gate resistor must also be considered. In order to determine the average power dissipated by the gate resistor, energy supplied to the capacitor is determined by:

21) $E = (2)(1/2) \bullet C_{GATE} \bullet V^2 = (Q_{GATE}/V) \bullet V^2 = Q_{GATE} \bullet V$

The factor of 2 comes from the fact that the gate must be both charged and discharged by the gate drive circuit. Each time the gate is charged or discharged, the gate drive circuit will dissipate an amount of energy which is equal to the amount of energy supplied to the gate. If we assume that the gate drive signal is running at 15kHz, the average power dissipated in the gate drive circuit is:

22) $P_{AVG} = E/T = (Q_{GATE} \bullet V)/T = Q_{GATE} \bullet V \bullet F = (110nC)(20.5V)(15kHz) = 34mW$

Obviously for this example power dissipation in the gate drive circuit is not a problem. However, for IGBTs with higher gate charge requirements, and higher operating frequencies, the power dissipation can become significant, and must be taken into consideration. To select the power rating of the gate resistor, assuming that all of the power in the gate drive circuit is dissipated in the gate drive resistor will lead to a conservative gate resistor rating. If a power resistor is required, it should have low inductance. A wirewound resistor is not recommended for this application, but if one is used, it must be noninductively wound.

The output of the UC3727 should be protected against adverse affects due to voltage overshoot on the gate drive signal by clamping the output circuit to both V_{CC} and V_{EE} with Schottky diodes. This is done in the circuit shown in Figure 9 with a UC3612 dual Schottky diode. For a detailed explanation of this problem see Unitrode Application Note U-111.

Once the gate drive resistor has been selected, the clamp level, clamp time, and desaturation amplifier blanking time must be selected. Choosing the clamp level involves a trade off between the soft turn on requirements and the short circuit characteristics of the IGBT. Basically the soft turn on requirements are derived from the reverse recovery characteristics of the free wheel diode if the IGBT is driving a clamped inductive load. Since the conductivity of the IGBT is reduced for lower gate voltage, the maximum current that the free wheel diode sees during reverse recovery can be controlled.

Since this example assumes a resistive load, the short circuit characteristics of the IGBT will determine the clamp requirements. Unfortunately, the short circuit characteristics are not always well known. Considerable effort must expended to test the device and determine a safe clamp level and clamp time. Test data has suggested that for the IGBT used in this example, a reduction in gate voltage to 10V will allow for a maximum short circuit time of about 40µs with a V_{DD} of 200V. With full 15V gate drive, the short circuit time would be 5µs worst case. However, a secondary requirement of the clamp circuitry is that the protection circuitry must be able to recognize that the device is back in saturation if the fault goes away during the allowable fault period. For a gate drive voltage of 8V, the APT50GL60BN will remain in saturation at the peak normal current load of 20A. Therefore 8V is chosen as a conservative number for the clamp level.

Once the clamp level is known, the only other constraint is that the DC impedance must be limited to approximately 10k ohms. With that in mind, referring to Figure 9 we have:

23) *(16.5V)(R14 /(R6 + R14)) = 8V*

24) *R6 + R14 = 10k*

A solution of R6 = R14 = 5.1k will satisfy the design requirements. The clamp input is also bypassed to common with 0.1µF as discussed in the output clamp section of this application note.

As previously detailed, the clamp time on the rising edge of the gate drive waveform is only important when driving clamped inductive loads. For purposes of this example, this time is arbitrarily chosen as 0.5µs. The blanking time for the desaturation amplifier is limited by the maximum allowable short circuit time under full gate drive voltage. This requirement stems from the fact that if a fault is present before the IGBT is commanded on, the UC3727 has no way of determining that the fault is present. Therefore, the IGBT will drive into the short circuit at full gate voltage for the duration of the blanking time. Since the maximum allowable short circuit time under these conditions is 5µs, the blanking time should be less, and 4µs was selected. Equations 7 and 8 can be solved simultaneously to obtain C12 = 100pF, and R7 = 91k.

DESIGN CONSIDERATIONS FOR THE FAULT CIRCUITRY

To program the fault circuitry, the short circuit characteristics of the IGBT are again used. The first consideration is the threshold of the desaturation comparator, which is programmed at the inverting input. For fast response, this trigger amplitude should be as low as possible. However, it must also be high enough to allow the comparator to recognize if a fault has gone away during the fault window. As detailed in the previous section, the IGBT will be operating under reduced gate voltage at that time.

The data sheets for the APT50GL60BN indicate that for a gate voltage of 8V, and collector current of 20A, the collector to emitter saturation voltage is 2V. Allowing for 1V of margin, plus a maximum diode drop of 1V, the DSAT- input is selected as 4V. The level is programmed by the voltage divider formed by R12 and R13, assuming the minimum level for V_{CC} of 15.5V. This leads to R12 = 18k and R13 = 51k.

The diode used in the fault circuit must be chosen for fast reverse recovery, low capacitance, and high breakdown voltage rating. **The reverse recovery time should be at least an order of magnitude faster than the short circuit time rating of the IGBT.** The capacitance should be low enough to prevent high currents from flowing into the DSAT- input in the presence of high dv/dt. Finally, the breakdown voltage rating must obviously be greater than the maximum IGBT collector voltage.

If the IGBT collector voltage is relatively low, the diode can be replaced with a high value resistor. This solution has the advantages of low capacitance and no reverse recovery problems. However, extreme care must be exercised to insure that the resistor is large enough to prevent the DSAT+ from overvoltage conditions formed by the resistive divider when the IGBT is off.

Another alternative for low power applications is to use a more conventional current sense resistor at the emitter of the IGBT. The DSAT+ input can be tied to the high side of the sense resistor, and the DSAT- input can be biased to some trip point proportional to emitter current. This allows for more precise control of the maximum current through the IGBT. Usually the voltage drop and power dissipation of the sense resistor are two high to make this a practical solution though. An example of this technique is shown in the examples section of this application note.

R10 is chosen to provide adequate bias current to the diode to insure that it is in the on state when the IGBT is in saturation. R11 provides isolation between the diode and the DSAT+ input. Its selection is fairly arbitrary, but the reverse recovery and capacitance characteristics of the diode must be considered to insure that excess current is not injected into the DSAT+ input during switching transitions.

The next consideration is the selection of the time the gate will be held at the clamp level in the presence of a fault, referred to as the fault window. Since the allowable short circuit time with a gate drive of 10V is 40µs, the fault window is selected as 10µs to allow for plenty of margin. The selection of the delay period should take into account the relative slow speed of optocouplers, and the timing requirements on the FRESET signal that must be provided to the UC3726. The blanking period is chosen as 100µs for this example. Using equations 9 and 10 this leads to:

25) $10\mu s = (R8)(C13) \bullet ln((R8 - 7600)/(R8 - 12400)$

26) $100\mu s = 0.4 \bullet (R8)(C13)$

These equations do not yield standard values when solved simultaneously. A close solution is C13 = 2200pF and R8 = 91k. This results in a fault window of 11.8µs and a blanking period of 80µs.

The only remaining programmable option selection is the fault window timing for the UC3726. This time duration must be long enough to allow for the slow speed of the optocoupler. For this example, the optocoupler (CNY17) has a typical switching time of 10µs. Choosing C3 = 2200pF and solving Equation 5 results in a fault window of 23µsec.

FILTER/DECOUPLING CAPACITOR CONSIDERATIONS

Proper bypass capacitor selection is essential to insure proper operation of the UC3726/UC3727 chip pair. The UC3726 does not have the high peak current requirements that the UC3727 does and therefore a high quality ceramic capacitor of about 1µF is usually sufficient. This capacitor must be located as close to the V_{CC} and GND pins of the chip as possible.

The UC3727 on the other hand must supply high peak currents during the charging and discharging of the IGBT gate. While all of the average current for the gate drive is ultimately supplied by the UC3726 through the pulse transformer, circuit inductances force most of the instantaneous peak current to come from the bypass capacitors. If insufficient bypassing is used, the ripple voltage at the UC3727 can be large enough to trip the under voltage lockout circuitry.

In order to determine the maximum allowable ripple voltage, Equation 6 is used. The margin allowed in Equation 6 becomes the maximum ripple voltage. Since the ripple voltage results from charging the IGBT gate, the equation leads to the bypass requirements for PV_{CC} and PV_{EE}:

27) $V_{ripple} = (V_A - V_B) - (V_{CC} + V_{EEUVLO} + 2V_D)$

The ripple voltage will be composed of a gate charge component and an ESR component. The gate charge component results from the voltage drop of the bypass capacitor due to gate charge requirements. The resulting voltage drop of the decoupling capacitor due to gate charge requirements is expressed as follows:

28) $dV_{CHARGE} = Q_G/C_{BYPASS}$

The ripple component due to ESR loss is directly proportional to the peak gate current. It is expressed as:

29) $dV_{ESR} = I_{PEAK} \bullet ESR$

In Equation 29, ESR represents the equivalent series resistance of the bypass capacitor. The sum of the voltage drops represented by Equations 28 and 29 must not exceed the maximum ripple voltage.

For the example shown in Figure 9, Equation 27 yields a maximum ripple voltage of 1.6V. The peak gate current is limited to 4A, and therefore we can calculate the maximum allowable ESR from Equation 9. If we use a maximum allowable ESR loss of 0.5V we have:

30) $ESR = 0.5V/4A = 0.125 \text{ ohm (max)}$

Allowing 0.5V for the charge component of the ripple voltage sets the minimum value of bypass capacitance:

31) $C_{BYPASS} = 110nC/0.5V = 0.22\mu F \text{ (min)}$

For this circuit a single 1µF capacitor on both the PV_{CC} and PV_{EE} pins of the UC3727 is sufficient. For larger values of gate charge the solution would involve a small ceramic capacitor for low ESR and a larger electrolytic capacitor in parallel to supply gate charge. To be conservative, a 10µF electrolytic capacitor is added between PV_{CC} and PV_{EE}. The V_{CC} and V_{EE} pins are also bypassed as described earlier in this application note and resistive isolation is provided between the high power and low power voltage supplies. R18 is added to balance the supply currents to ensure active start up in the presence of slowly rising supply voltages. These equations only describe the minimum bypass requirements. If the system is particularly noisy, significantly more bypass capacitance may be required.

TEST CIRCUIT RESULTS

The example circuit was built and tested to verify operation, with the results shown in Figure 10. The waveforms for V_E and I_E are shown. Notice the characteristic "tail" in the turn off waveforms for both current and voltage. The tail results from the fact that IGBTs are minority carrier devices, and therefore have stored charge. At the beginning of turn off, the collector to emitter current decreases rapidly to the level of the hole recombination current for the device. At this point di/dt decreases, and the voltage and current waveforms tail off at a much slower rate. The reason for the bump in the voltage waveform is that as di/dt decreases, inductive voltage drops also decrease, and therefore

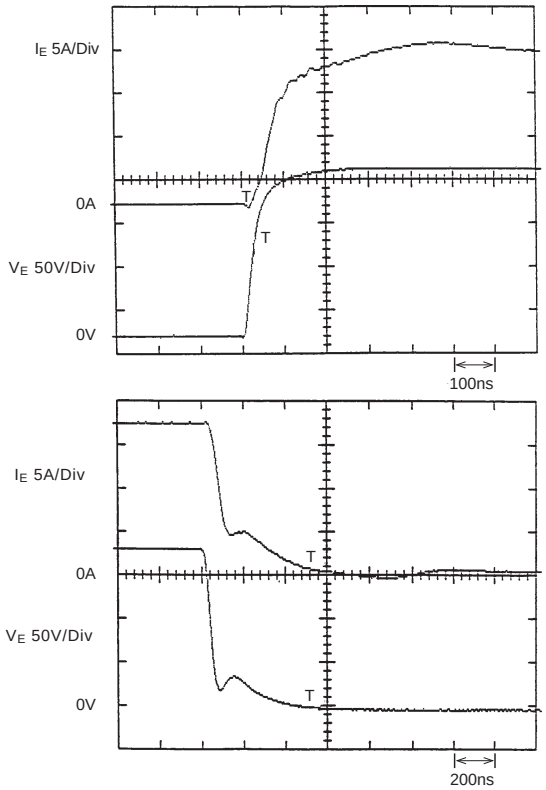

Figure 10. Test Circuit Waveforms (V_{PD} = 375V)

more voltage is dropped across the IGBT at the start of the tail.

Figure 11 shows waveforms for the same circuit when tested with V_{DD} = 375V. Notice the slower switching times due to the higher output voltage and current.

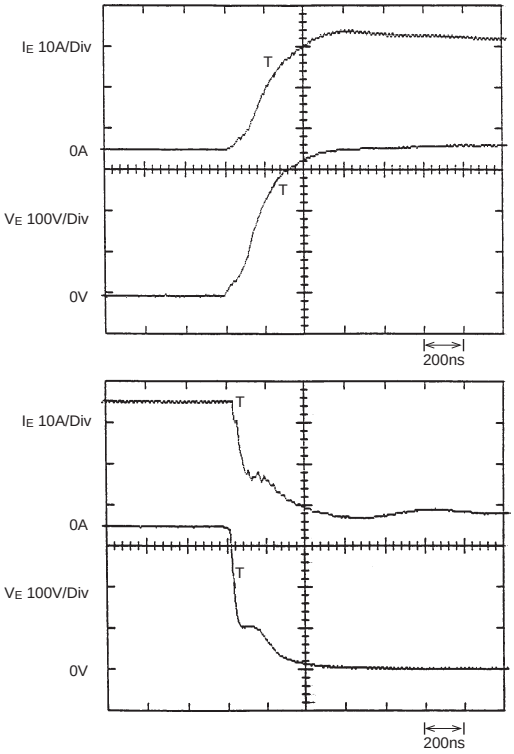

Figure 11. Test Circuit Waveforms (V_{PD} = 375V)

DESIGN EXAMPLES/APPLICATIONS

The example circuit described earlier in this application note provides a good baseline for calculating component values for the required support circuitry for the IGBT driver pair. Many other circuit topologies can be used with this chip set, and the same general rules apply as for the example circuit. The individual system designer must evaluate the particular requirements, and make component selections accordingly. This section illustrates some general circuit topologies which may be encountered by a typical system designer.

SENSING FAULTS WITH A CURRENT SENSE RESISTOR

Figure 12 shows a way of detecting faults with a current sense resistor. The desaturation comparator is used to detect over current conditions. Using a resistor divider network from V_{CC} allows the trip level to be set at the D_{SAT-} input to the comparator. Current is sensed at the emitter of the IGBT, with the filtered voltage across the current sense resistor fed into the D_{SAT+} input. This approach has an advantage for low power applications because there is no diode in the protection circuit and therefore no reverse recovery problems to worry about. Also with this technique, more precise control of the current limit is possible. A drawback to this approach is that the filter time constant required may be too long for IGBTs that can not tolerate fault conditions for very long. Also, for high power applications the power requirement for the sense resistor may be impractical.

HALF BRIDGE OUTPUT CIRCUIT

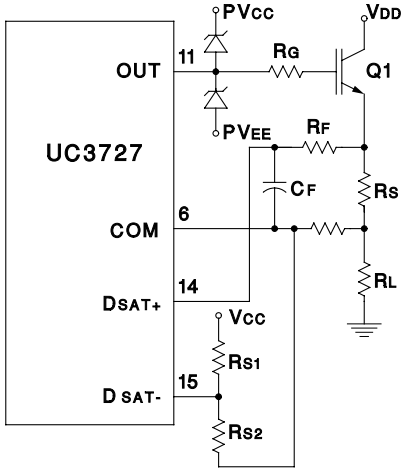

Figure 12. Detecting Faults with Current Sense Resistor

Figure 13 shows a half bridge output circuit with a dual secondary transformer. The low side of the bridge is driven by a UC3727 with its polarity reversed from the upper side driver. Cross conduction is controlled by providing dual gate resistors for both upper and lower IGBTs. Carefully selecting RG1 and RG2 can provide fast turn-off and slow turn-on. If more accurate dead time between on commands for upper and lower IGBTs is required, the ENBL inputs can be used. Using an optocou-

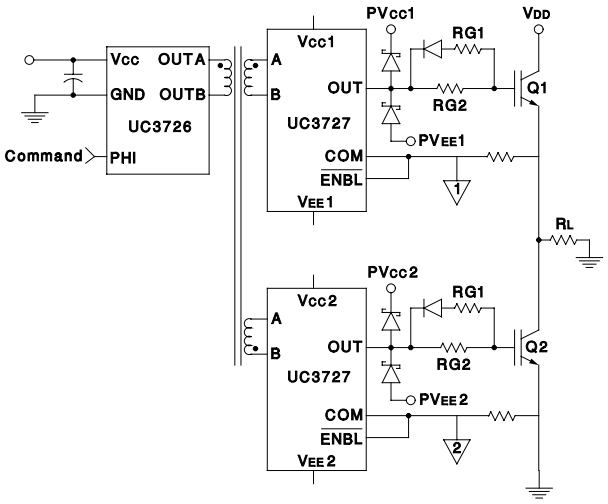

Figure 13. Half Bridge Output Circuit

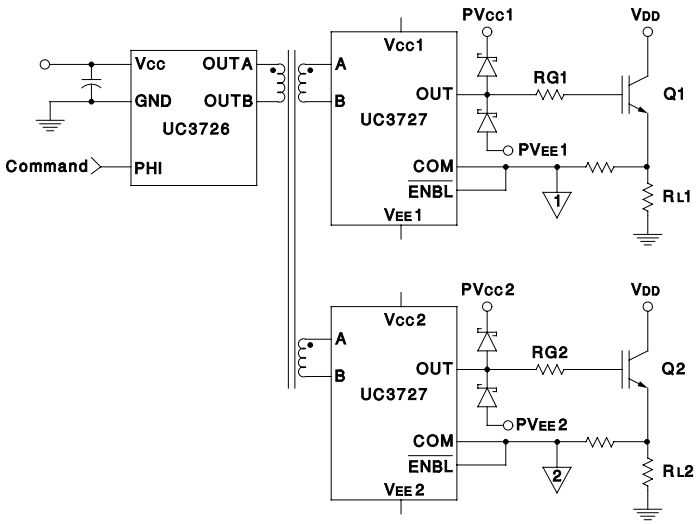

Figure 14. Dual High Side Driver Circuit

pler or level shift network, the $\overline{\text{ENBL}}$ input can be controlled separately to assure that cross conduction is prevented.

MULTIPLE ISOLATED DRIVER CIRCUIT

Figure 14 shows a dual isolated driver circuit topology. By using a multiple secondary winding transformer, several IGBTs can be driven simultaneously. Isolation, command signal, and power are provided to each IGBT by the single transformer. Obviously power dissipation in the UC3726 is a consideration, and ultimately will be a limiting factor in determining the maximum number of IGBTs that can be driven. The $\overline{\text{ENBL}}$ inputs can also be used to provide dead time between IGBTs if it is required.

UC3726/UC3727 IGBT EVALUATION KIT

Unitrode Integrated Circuits has designed an evaluation kit which can be used to demonstrate the UC3726/UC3727 IGBT driver pair. The kit consists of a custom PC board, two each of the UC3726 and UC3727, a UC3612 Schottky diode pair, and one Coilcraft Q3868-A transformer. The purpose of this evaluation kit is to provide the user with a way of quickly demonstrating the driver pair for an individual application.

The schematic, silkscreen, and artwork for the evaluation board are shown in Figures 15, 16, 17, and 18 respectively. The schematic for the evaluation board is identical to the schematic shown in the example circuit (Figure 9), except for some additional components which may be required to evaluate certain conditions.

Table 1 shows the list of materials for the demo board for building the example circuit. If it is desired to evaluate other requirements than those described in this application note, the same equations should be used to determine component values. For more information on obtaining this demo kit, contact Unitrode Integrated Circuits at (603) 429-8610.

SUMMARY

By utilizing the new UC3726/UC3727 IGBT driver chip pair, a practical and cost-effective solution to the problem of driving high-side IGBTs can be realized. This chip pair incorporates several special features to provide fault protection and optimum gate drive. Using a high voltage isolation transformer precludes the need for high voltage integrated circuits. This chip pair is ideally suited for a wide range of isolated IGBT driver applications.

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Coilcraft telephone number : 1-800-322-COIL

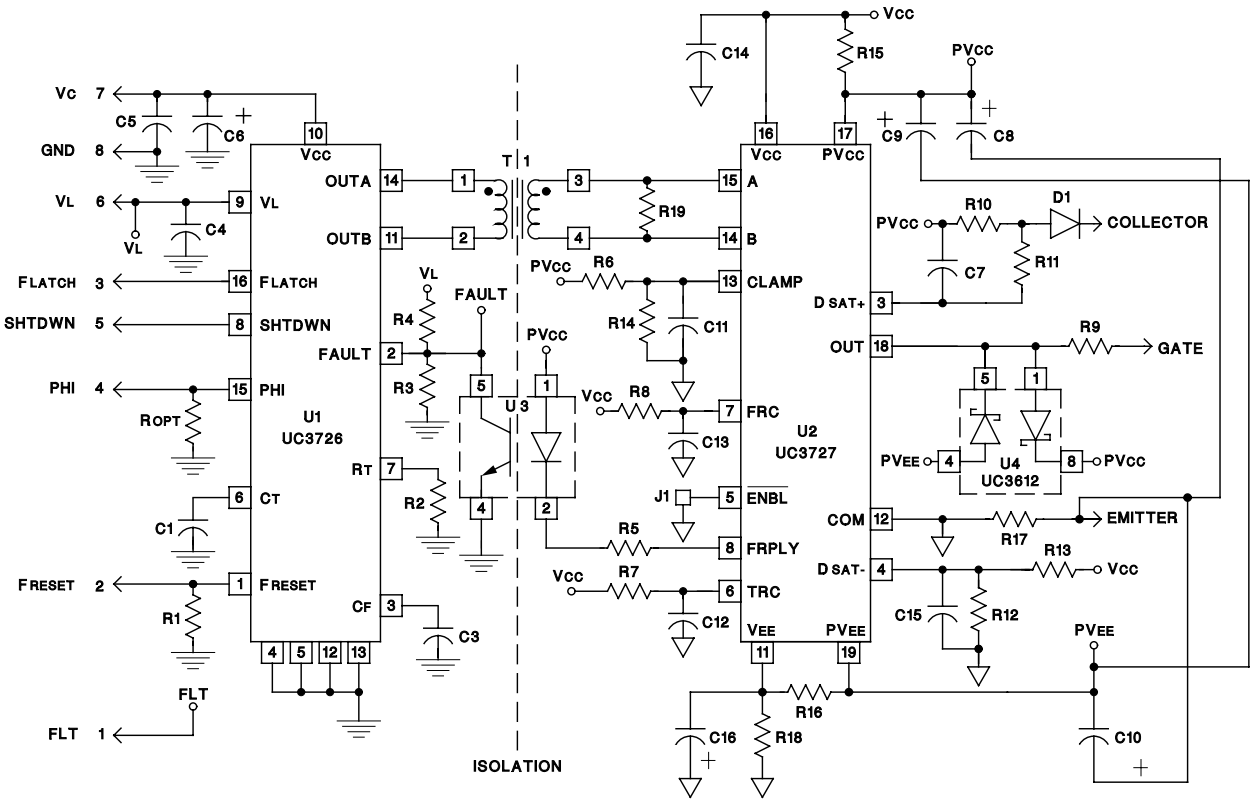

Figure 15. IGBT Driver Pair Evaluation Board Schematic

TABLE 1

UC3726/UC3727 IGBT ISOLATED DRIVER PAIR DEMO KIT

LIST OF MATERIALS

CAPACITORS

C1, C12	100pF, 35V
C3, C13	2200pF, 35V
C4, C11	0.1µF, 35V
C5, C8, C10	1µF, 35V
C14, C16	1µF, 35V
C6, C9	10µF, 35V

DIODES

D1	UF4007, BV= 1000V (General Instrument)

INTEGRATED CIRCUITS

U1*	UC3726Isolated Drive Transmitter
U2*	UC3727Isolated High Side IGBT Driver
U3	CNY17 Optocoupler, 10µs
U4*	UC3612 Schottky Diode Pair

R1, R8, R11, Ropt	2k, 1/4W
R2, R4, R6, R14	5.1k, 1/4W
R5	10k, 1/4W
R7, R8	91k, 1/4W
R9	5.6Ω, 1W
R10, R12	18k, 1/4W
R13	51k, 1/4W
R15, R16, R17	3.3Ω, 1/4W

MAGNETICS

T1*	Coilcraft Q3868-A

*Included with demo kit.

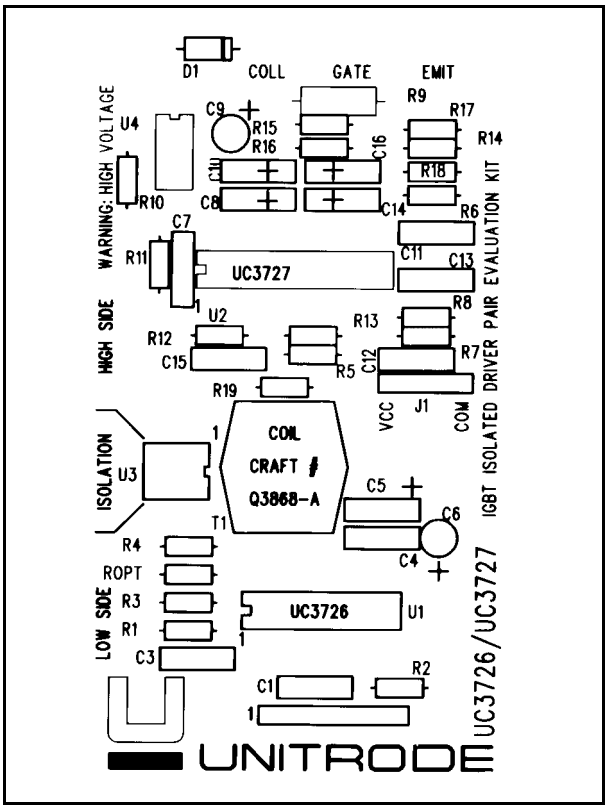

Figure 16. Silkscreen

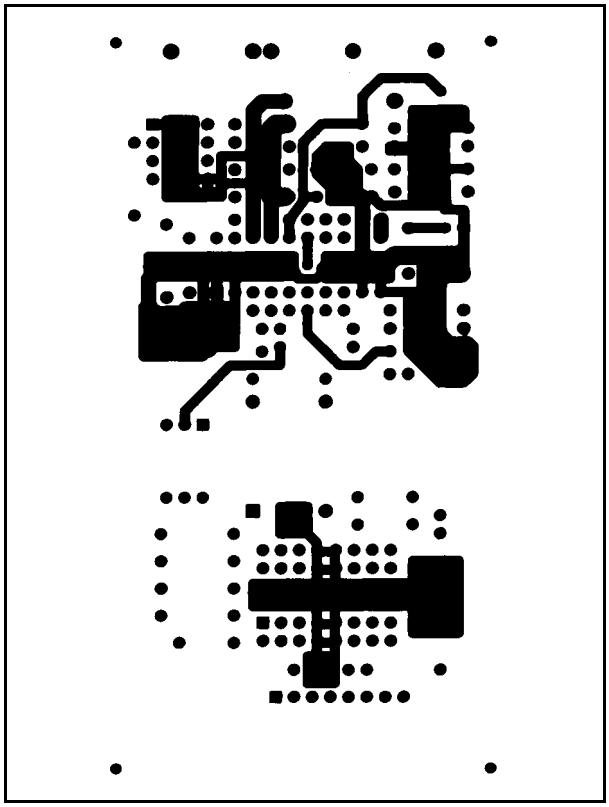

Figure 17. Component Side

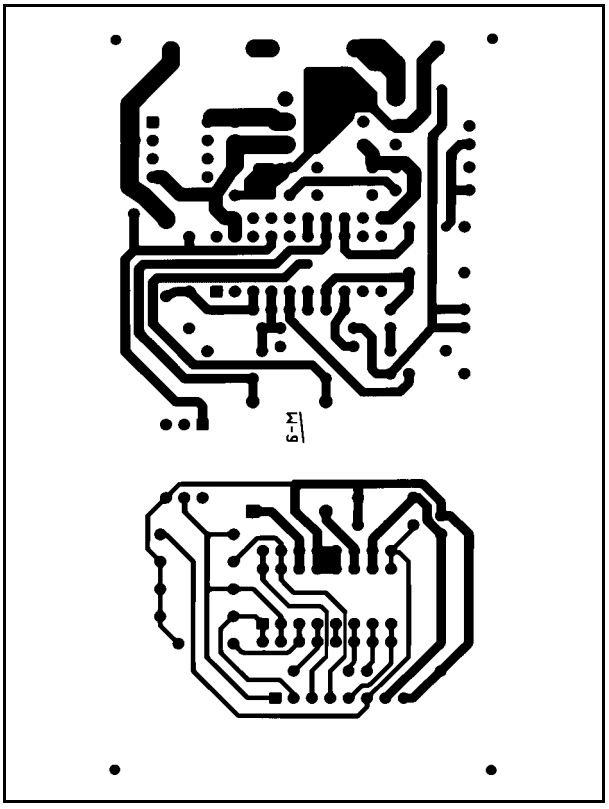

Figure 18. Solder Side

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